RĂZVAN GABRIEL PREJBEANU

RĂZVAN GABRIEL PREJBEANU

- DIGITAL ELECTRONICS – LAB - BASED ACTIVITY

Editura UNIVERSITARIA
Craiova, 2023

Referenți științifici:

Prof.univ.dr.ing. Dan Selișteanu
Prof.univ.dr.ing. Dorin Șendrescu

Descrierea CIP a Bibliotecii Naţionale a României
PREJBEANU, RĂZVAN GABRIEL
Digital electronics - Lab-based activity / Răzvan Gabriel Prejbeanu. - Craiova : Universitaria, 2023
Conţine bibliografie
ISBN 978-606-14-1936-4

004
62

1. EXPERIMENT 1
Presentation of the laboratory platform

1. The purpose of the laboratory assignment

The paper aims to present and test the platform of the Digital Electronics laboratory, basic teaching material used not only in carrying out the laboratory works contained in this guide, but also in the scientific research activity in the field.

2. Theoretical aspects

2.1. Description of the laboratory platform

The laboratory platform consists of the multifunctional platform and mounting platform equipped with connectors for integrated circuits.

2.1.1. Description of the multifunctional platform

The multifunctional platform, plate M, consists of an assembly of two overlapping plates, electrically interconnected and stiffened from the point of view mechanically by means of connectors.
The multifunctional platform contains several blocks with well roles defined, visible in plate M and in the drawing presented in figure 1.

The upper plate, plate 1, represents the aesthetic face of the platform on which the component blocks of the assembly and where they are are grouped and inscribed plant the pins for connections, the microswitches for power, the keys of also controls the four “7 - segment digits” of the display block.
The lower plate 2, is the one on which most of them are planted electronic components: integrated circuits, transistors, LEDs, resistors, capacitors, etc.

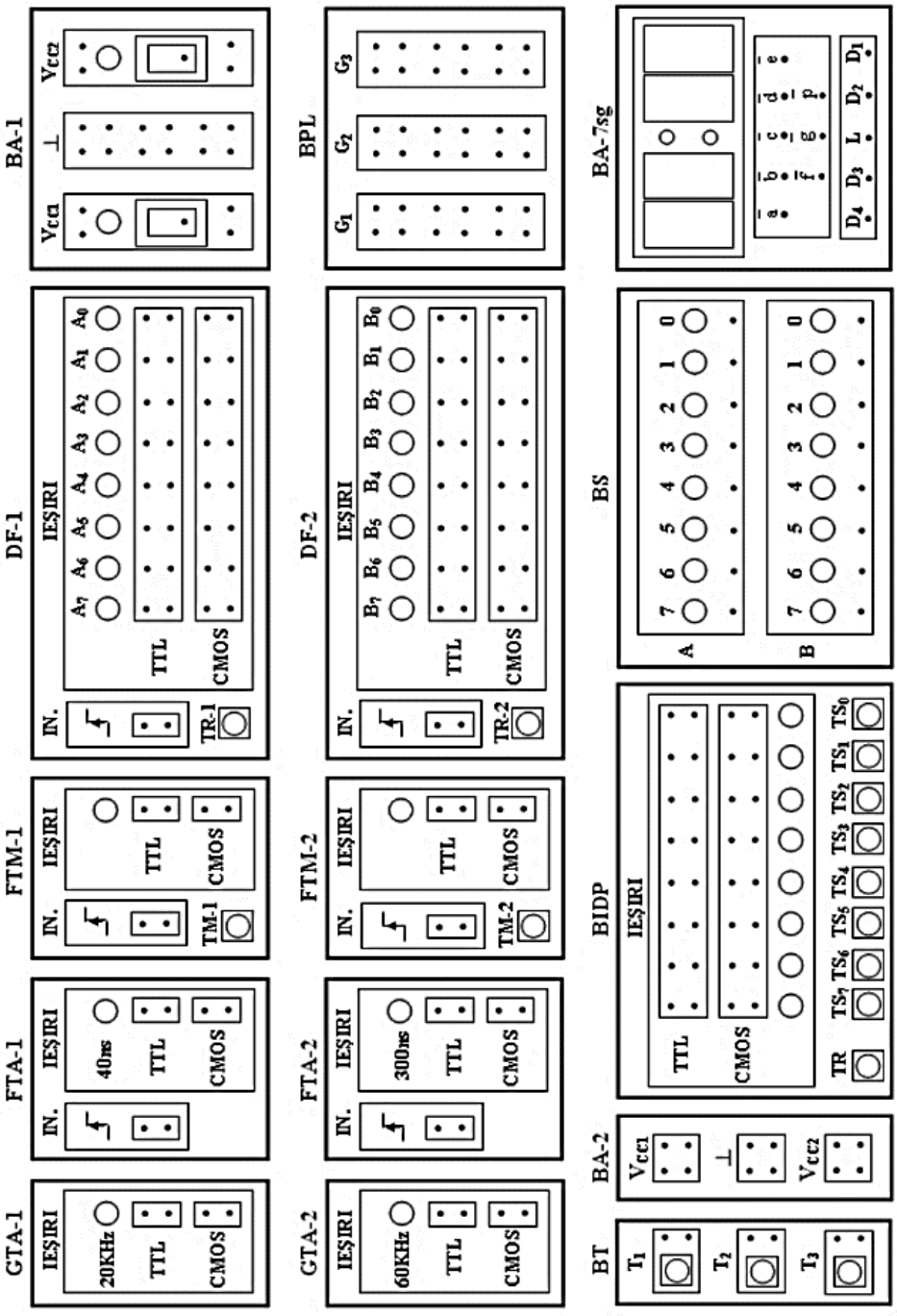


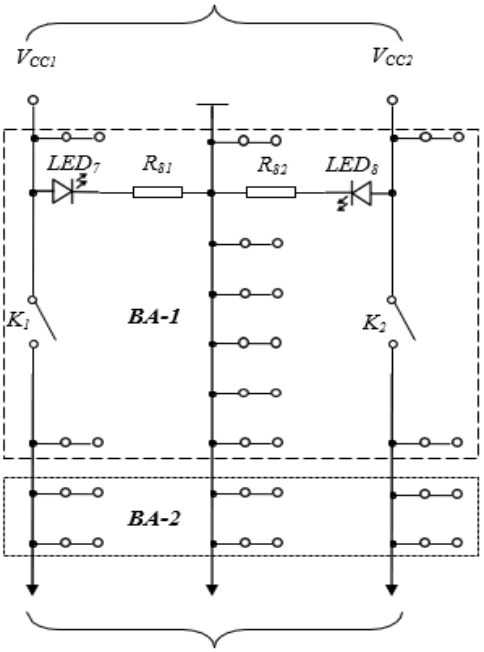
Figure 1. General view of the test platform, plate M (main)

2.1.1.1. Description of the power supply unit

The power block, figure. 2, consists of sections BA-1 and BA-2, characterized by the areas related to the two supply voltages V_{CC1} (5V / 1A) and V_{CC2} (15V / 1A), as well as the common ground of the entire assembly.

The BA-1 block contains two signaling circuits, equipped with LEDs, which indicate the presence of the two voltages at the entrance to the platform, two microswitches for coupling these voltages and a series of pins for making connections in case of need. BA-2 is an extension of BA-1, placed diagonally from it and containing only connection pins. Depending on the specific situations that may arise, the assembly platform can be fed from either BA-1 or BA-2.

From the stabilized voltage sources in the panel



To the circuits of the multifunctional platform

Figure 2. Power block diagram

2.1.1.2. Description of the block of automatic clock generators

The block of automatic clock generators consists of sections GTA-1 and GTA-2, figure 3, which generate clock pulses with frequencies of 20kHz and 60kHz, respectively, and the waveforms shown in figure 4.

The only difference between the two GTAs lies in the value of the capacitance (C_1*=100nF*, while C_2*=33nF*) that enters the period calculation

formula:

$$T_i \cong 1{,}29 \cdot R_{1(6)}\, C_i, \text{ cu } i=1,2.$$

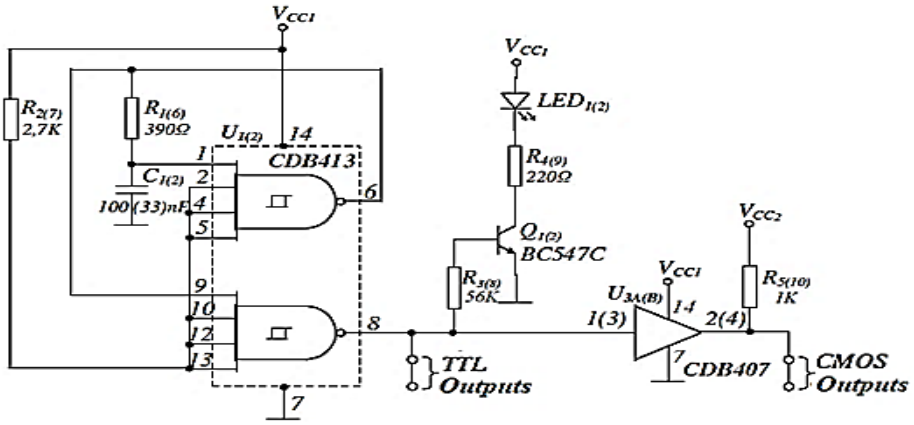


Figure 3. Scheme of GTA-1(2) automatic clock generators

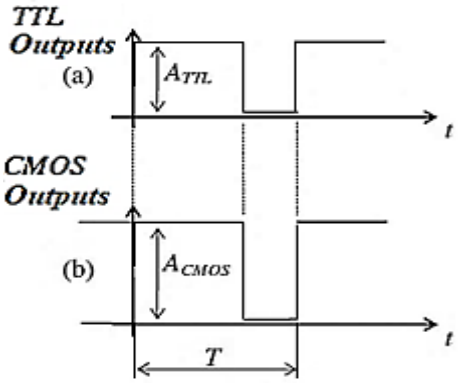


Figure 4. Output signals of GTA-1(2)

The frequency of the output signals is calculated with the relations:

$$f_1 = \frac{1}{T_1} = 20kHz \text{ and } f_2 = \frac{1}{T_2} = 60kHz$$

The scheme of a GTA consists of a rectangular voltage generator made with the integrated circuit CDB413 that contains two NAND gates - Schmitt trigger whose use gives very good edges to the generated pulses, a signaling circuit equipped with LEDs and a TTL-CMOS interface circuit, actually a buffer with an empty collector, made with 1/6 of the CDB407 integrated circuit (see the appendix, fig. A3), with the role of voltage level adapter.

A pair of pins is provided for the TTL and CMOS outputs.

2.1.1.3. Description of the automatic clock formers block

The block of automatic clock formers is composed of FTA-1 and FTA-2, figure 5, both controlled on the rising edge of the pulses applied to the inputs and generating at the outputs pulses with standard durations of *40 ns* and *300 ns* respectively (see the diagrams in figure 6), due to the different values of the capacities C_3=*47pF* and C_4=*360pF* that enter into the relationship for calculating the pulse duration:

$\tau_i \cong 0,7 \cdot R_{11(15)} C_i$ cu i=*3, 4.*

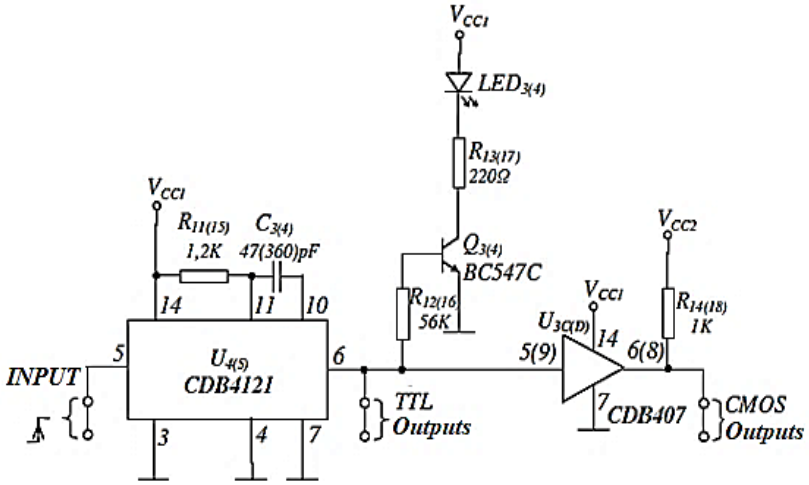


Figure 5. Schematic of automatic clock formers FTA-1(2)

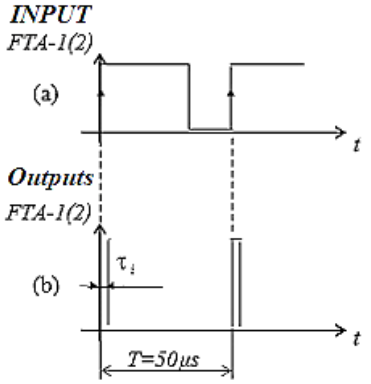


Figure 6. Explanation for the operation of FTA-1(2)
a) the input signal; b) the output signal

In figure 6 it was assumed that FTA-1(2) are commanded by GTA-1 which generates rectangular pulses with a frequency of *20kHz* and a period

$T=50\mu s$.
Each of the two formers contains a CDB4121 monostable toggle circuit, a signaling circuit and a TTL-CMOS interface circuit.
A pair of pins is provided for the TTL and CMOS outputs.

2.1.1.4. Description of the block of manual beat generators

The two formers are identical and receive at the inputs the rising fronts of the pulses resulting from the operation of the TM-1(2) keys, FTM-1 and FTM-2, figure 7, generating at the outputs pulses with standard durations of approx. 0.25s (see diagrams in figure 8).
The pairs of pins provided at the FTM-1(2) inputs allow the use of these circuits also as automatic clock generators or timing circuits in various applications.

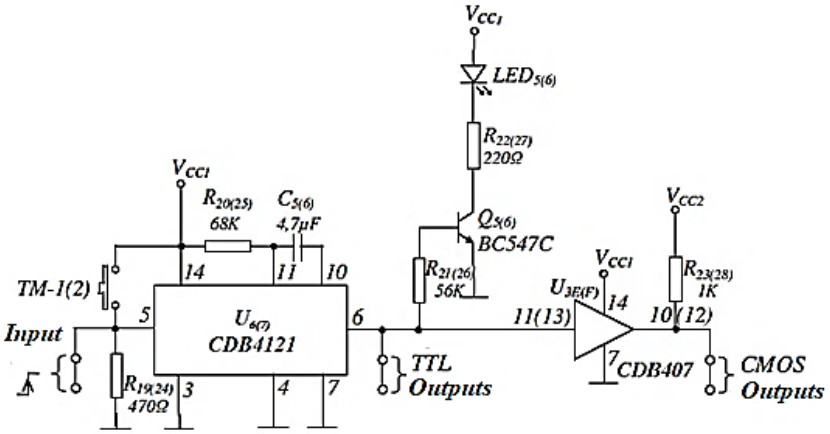


Figure 7. Schematic of manual clock formers FTM-1(2)

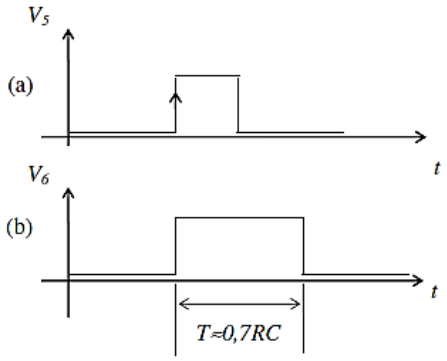


Figure 8. Explanatory for the operation of FTM-1(2)

a) the input signal; b) the output signal

Each of the two formers, made with one CDB4121 monostable toggle circuit are equipped with one LED signaling circuit, one interface circuit and one pair of pins for each type of output: TTL and CMOS.

2.1.1.5. Description of the block of frequency dividers, DF-1 and DF-2, figure 9.

The frequency dividers are ordered on the rising edge of the pulses and allow counting in binary, on 8 bits, the pulses applied to the inputs. They are made of two CDB4193 4-bit counters connected in cascade, each of which consists of 4 bistable flip-flops.

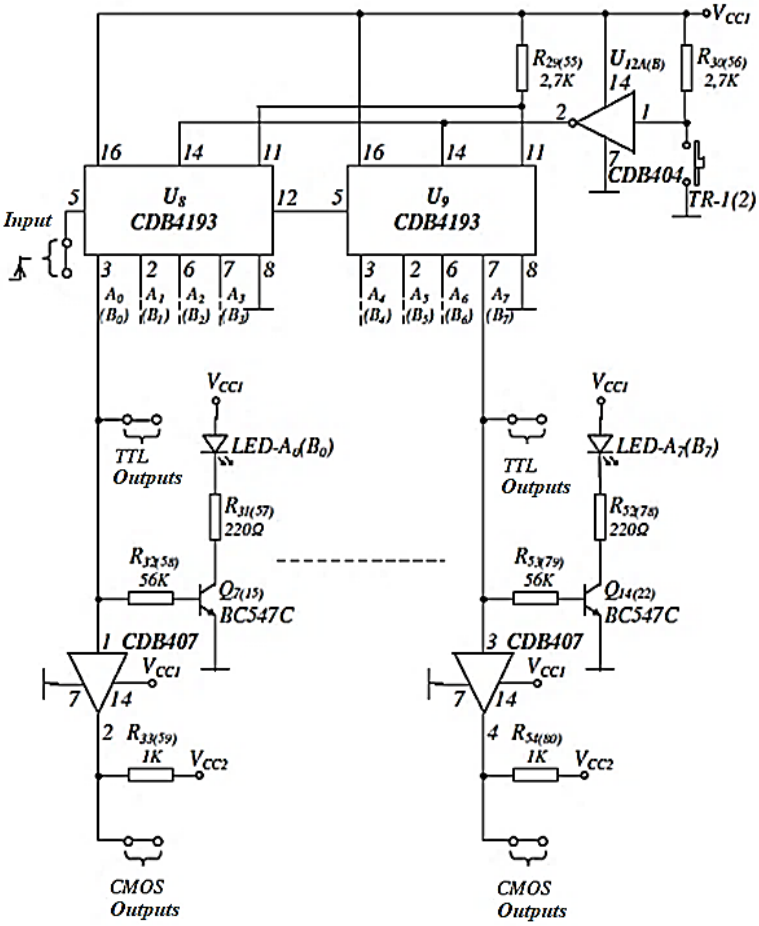


Figure 9. Schematic of frequency dividers DF-1(2)

The frequency dividers also contain an inverter (from the structure of the CDB404 integrated circuit) and a Reset key - TR-1(2) required to initialize the scheme (delete the information from the bistable flip-flop cells) after

connecting the supply voltage or after another use previous of the respective circuits.

An LED signaling circuit, a TTL-CMOS interface circuit and a pair of pins for each type of output: TTL and CMOS are connected to each of the 8 outputs of the frequency dividers.

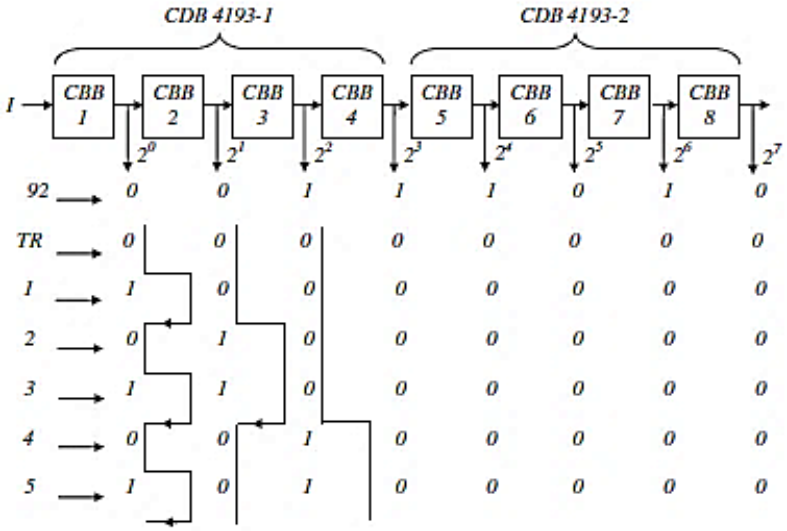


Figure 10. Explanatory for the operation of DF-1(2)

2.1.1.6. Description of the block of free pins

The block of free pins (BPL), figure 11, consists of 3 groups of 12 pins short-circuited between them within the group and having the role of allowing, when necessary, the multiplication of some contacts.

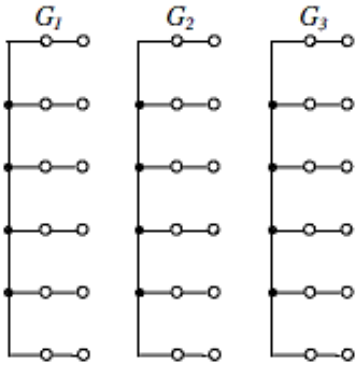


Figure 11. Block of free pins

2.1.1.7. Description of the key block

The key block (BT), figure 12, contains keys T1, T2 and T3, available through the related pins for use in various circuits.

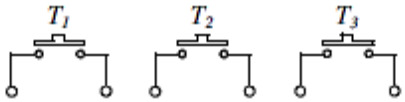


Figure 12. Key block

2.1.1.8. Description of the parallel data entry block

The parallel data entry block (BIDP), figure 13, consists of 8 bistable SR flip-flop circuits made with NAND gates from the CDB400 integrated circuit structure, 8 registration keys (TS_0, TS_1, ..., TS_7), one each for each SR bistable toggle and a general clear (TR) key.

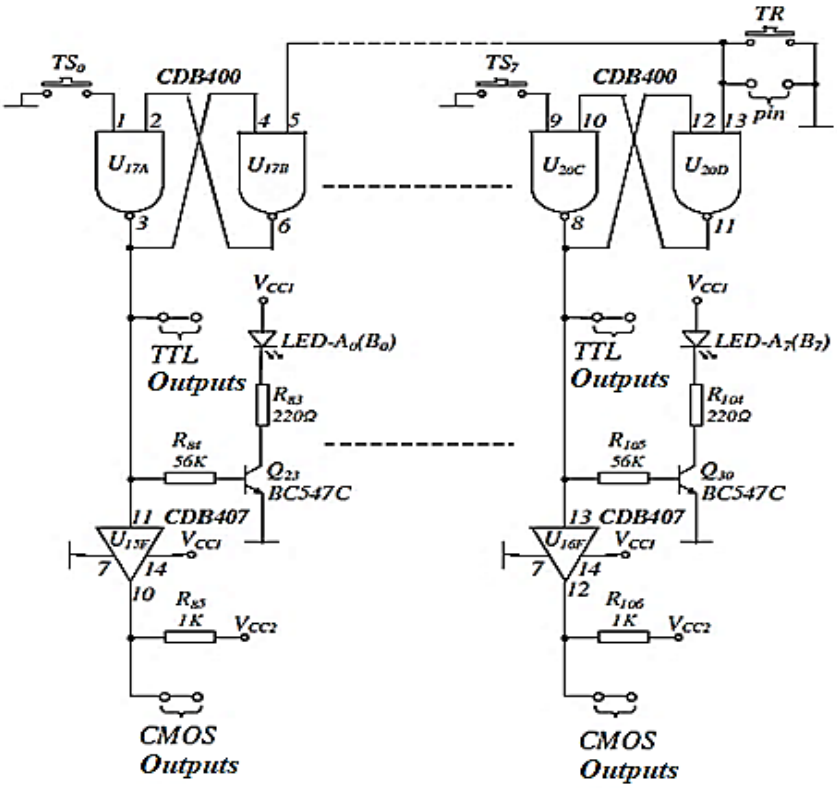


Figure 13. Parallel data entry block

BIDP allows the provision of 8-bit words, viewable by LED-equipped signaling circuits and available with TTL and CMOS levels on specially allocated pin pairs.

2.1.1.9. Description of the signaling block

The signaling block (BS) consists of two sections, A and B, figure 14, each with 8 signaling circuits equipped with LEDs. The existing pins under each of the 16 LEDs, see figure 1, represent the inputs to the respective signaling circuits.

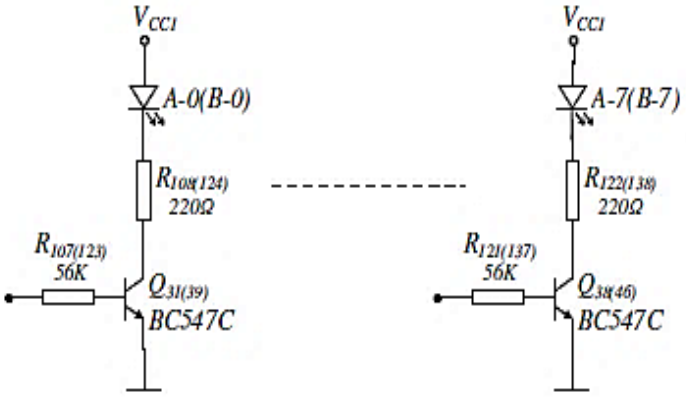


Figure 14. Scheme of sections A(B) of the BS block

2.1.1.10. Description of the 7-segment display block

The 7-segment display block (BA-7sg), figure 15, consists of 4 displays with 7 segments of the MDE2101R type, figure 16 a, in common anode connection, see the electrical diagram in figure 16 b.

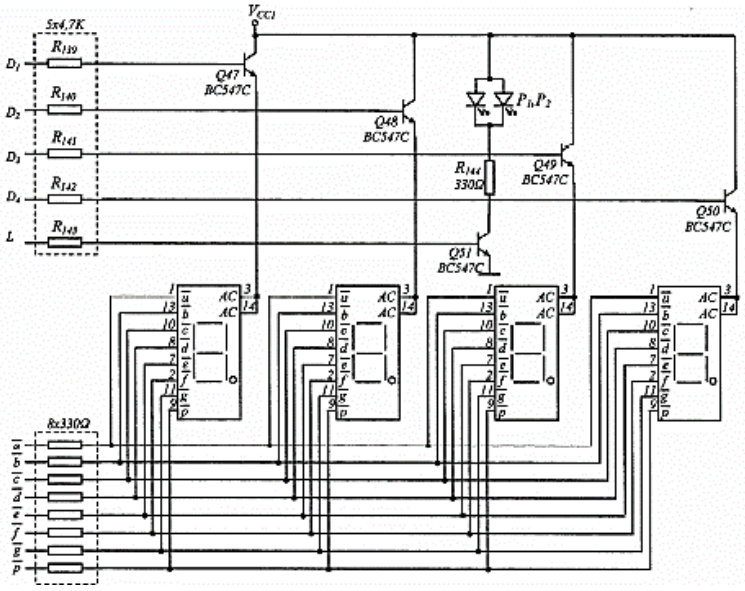


Figure 15. Schematic of the 7-segment display block

The 4 displays -s are grouped by two, see figure 1, the two groups being separated by two vertically arranged LEDs.
The homologous segments of the displays are interconnected, accessible to the external pins $\bar{a}$, ... $\bar{p}$ and can be activated with logic 0.
The displays and the group of two LEDs are powered by
through transistors Q_{47}, ..., Q_{51}, figure 15, can be activated with logic 1 at pins D_1, D_2, L, D_3 and D_4.

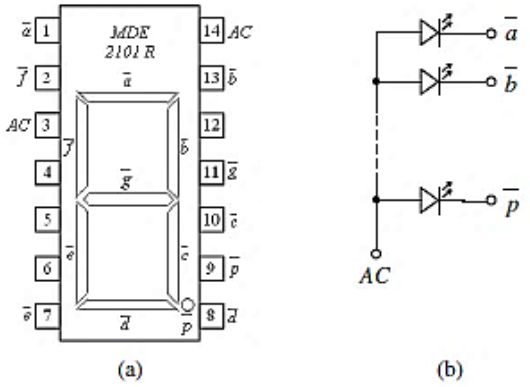


Figure 16. Scheme of a 7-segment display
a) How to connect the segments to the pins; b) Electrical diagram

The block is designed to be used in various applications, from the simplest to complex applications such as multiplexed display.

2.1.2. Description of the mounting platform

The mounting platform, plate 3, is equipped with circuit bars integrated and a large number of pins connected to these bars and which allow interconnection of integrated circuits and other possible electronic components. For an easier use of the mounting platform, a grid with appropriate cutouts, which allows the corresponding pins to be numbered of the strips in accordance with the number of pins of the integrated circuits used.

3. Procedure of work progress

Testing the multi-functional platform

3. 1. Power block testing

a) Check the "open" state of switches K_1 and K_2 in BA-1;

b) Insert the connector of the multifunctional platform into its pair on the side of the electrical panel between the tables;

c) Switch on the switch key related to the work table in the electrical panel;

d) LEDs 7 and 8 will light up, indicating the presence of voltages V_{CC1}, V_{CC2} and of the mass in the platform, but only before K_1 and K_2, see figure 1, 2;

e) Measure the voltages V_{CC1} and V_{CC2} with respect to ground with a voltmeter;

f) The switch K1 is switched on, sending the voltage V_{CC1} throughout the multifunctional platform, except in the collectors of the transistors in the buffers with an empty collector;

g) It is noted that some of the LEDs in the signaling circuits of the DF-1, DF-2 and BIDP blocks, as well as those of the GTA-1 and GTA-2 blocks;

h) DF-1, DF-2 and BIDP are reset, the only LEDs on the platform that remain lit are those of BA-1 and those of GTA-1 and GTA-2. The reason why the latter remain lit has been discussed previously;

i) The switch K_2 is connected, which sends the voltage V_{CC2} to the collectors of the transistors in the empty-collector buffers.

3.2. Testing the block of automatic clock generators

a) Connecting a two-channel oscilloscope between one of the TTL or CMOS outputs of the GTA-1 and ground, the waveforms in figure 4;

b) The period T of the GTA-1 oscillations is determined, making the product between the number of divisions on which T extends and the time/division displayed by the oscilloscope;

c) Determine the frequency f of the oscillations with the relationship f = 1/T and verify that it is close to 20 kHz;

d) The A_{TTL} amplitude of the oscillations is determined, making the product between the number of vertical divisions and the voltage scale displayed by the oscilloscope;

e) The A_{CMOS} amplitude of the oscillations is determined in the same way as in point (d);

f) Repeat the experiments from points (a) ... (e) for GTA-2.

3.3. Testing the automatic clock formers block

a) The TTL output of the GTA-1 is connected to the FTA-1 input with the help of a single connection;

It is recalled that such a coupling would normally require two connections (hot wire and ground), but since the multifunctional platform has common ground for all circuits, only one connection is sufficient.

b) Connect the probe corresponding to channel 1 of the oscilloscope to the FTA-1 input and the second probe – to the TTL output of the same circuit. The waveforms in figure 6 are visualized;

c) By moving the second probe to the CMOS output of FTA-1, the waveforms are visualized and compared with those obtained at point (b);

d) Repeat the experiments from points (a) ... (c) for FTA-2.

3.4. Manual clock former block testing

a) Without making any additional connection, TM-1 is pressed and it is found that the LED in the signaling circuit at the output of FTM-1 remains lit for a time interval greater than the one in which the key was pressed. The diagrams in figure 8 are justified in this way;

b) The experiment from point (a) is repeated for FTM-2.

3.5. Frequency divider block testing

a) Put the frequency divider in counter mode controlled by manual clock, connecting the TTL output of FTM-1 to the input of DF-1;

b) DF-1 is reset by activating TR-1;

c) By repeatedly pressing the TM-1 key, it is verified, with the help of the signaling circuits in DF-1, that it counts correctly;

d) Connect the input of DF-1 to the input of FTM-1, i.e. connect the input of DF-1 directly to the TM-1 key (see diagram in figure 7);

e) Press the TM-1 key repeatedly and check that DF-1 counts incorrectly due to parasitic impulses introduced by the key;

f) Connect the TTL output of GTA-1 to the input of DF-1;

g) DF-1 is reset;

h) All 8 LEDs in the signaling circuits of DF-1 are found to be permanently lit. In reality, they pulse with a very high frequency and the eye perceives them as being permanently lit;

i) Place the probe corresponding to channel 1 of the oscilloscope on the input pin of the first bistable in the DF-1 structure, and the other probe on pin A_1 from the output of the same bistable. The double period of the pulses from the output of the bistable is observed, so the frequency is half that of the pulses applied to the input.

j) Repeat the experiment from point (i) for the CMOS outputs and highlight the differences that appear;

k) With GTA-1 connected to the input of DF-1, cascade the frequency divider DF-2 (TTL A7 output of DF-1 to the input of DF-2) with DF-1. A 16-bit counter is thus created, where the last 7 bits pulse with a lower and lower frequency as we move from B_1 to B_7.

Frequency counting and dividing operations are now obvious.

3.6. Testing the block with free pins

The voltage V_{CC1} is successively brought to one of the zones G_1, G_2 and G_3 and the existence of a logical "1" on each of the 12 pins of each zone is verified with one of the signaling circuits of the BS.

3.7. Testing the key pad block

a) One of the terminals of the T_i keys, with $i=1, 2, 3$, is successively connected to V_{CC1}, and the other terminal is connected to one of the 16 signaling circuits in the BS;

b) Press the T_i key and check that the LED in the respective signaling circuit lights up.

3.8. Testing the parallel input block

a) Press the RESET key, *TR*, so that all 8 bistables of the block are set to zero;

b) Press the TS_i keys and get the desired binary configuration on the BIDP byte, visualized on the 8 LEDs;

c) The bistables are reset by pressing the *TR* key.

3.9. Testing the signaling block

a) Connect a connection wire to V_{CC1} (logic 1) and touch the other end of the wire to the input pins of the 16 signaling circuits. The successive lighting of the 16 LEDs is observed;

b) With the connection wire connected to ground (logical 0) the experiment from point (a) is repeated. All LEDs are found to remain off.

3.10. Testing the 7-segment display block

a) The pins $\bar{a}$, $\bar{b}$, ..., $\bar{p}$, are connected in order to the TTL outputs of the BIDP, from rank 20 to rank 27;

b) Pins D1, ..., D4 are connected to outputs B0, ..., B3 of DF-2, set to counter mode controlled by manual clock (DF-2 input coupled to FTM-2 TTL output);

c) TM-2 is successively operated and all segments and points are visualized on the 7-segment displays;

d) TS0, ..., TS7 are successively activated and the successive deactivation of segments $\bar{a}$, $\bar{b}$, ..., $\bar{g}$ and finally points $\bar{p}$ is noted;

e) The BIDP is reset by pressing the TR key and it is noted that all the segments and points are lit again on the 4 displays.

3.11. Procedure:

3.11.1. Connect the platform kit to ac power supply.
3.11.2. Connect the NOR gates for any of the logic functions to be realised.
3.11.3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
3.11.4. Apply various input combinations and observe output for each one.
3.11.5. Verify the truth table for each input/ output combination.
3.11.6. Repeat the process for all logic functions.
3.11.7. Switch off the ac power supply.

RESULT: NAND & NOR are verified as universal gates successfully.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch free and uninsulated wires.

2. EXPERIMENT 2
The analysis and synthesis of combinational logic circuits

1. Theoretical aspects

This laboratory work aims to present the problems related to the analysis and synthesis of a simple combinational logic circuit.

The combinational logic circuits (c. l. c.) are circuits without memory, characterized by the fact the logic values of the output functions depend only on the logic values of the input variables, those being independent of the previous states of the circuit.

The block diagram of a c. l. c. is given in the fig. 17, the output functions can be written as:

$$Y_k = Y_k(x_1, x_2, ..., x_n), \text{ with } k = 1, 2, ..., m. \quad (2.1)$$

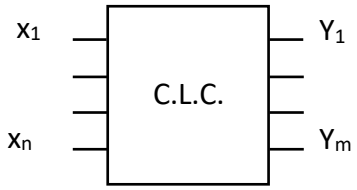


Figure 17. Block scheme of a c. l. c

The c. l. c. analysis starts with the known logic diagram of the circuit and aims to establish its operating module either by building the operating table or by writing the analytical form of the output function.

The c. l. c. synthesis starts from the function that the circuit must fulfill and aims to obtain a (minimal) variant of its structure.

For instance, given the function

$$Y = A \oplus B \quad (2.2)$$

and the truth table of the XOR function:

Tab. 2 The (truth) function table of XOR

B	***A***	***Y***
0	0	0
0	1	1
1	0	1
1	1	0

The c. l. c synthesis represented by the relation (2.3) and Tab. 2.

The FCD is:

$$Y = \overline{A}B + A\,\overline{B} \tag{2.3}$$

We have the conjunctive canonical form (FCC):

$$Y = (A + B)\,(\overline{A} + \overline{B}) \tag{2.4}$$

By adding to the FCD the (2.2) relation, $A\overline{A}=0$, $B\overline{B}=0$ we get:

$$Y = A \oplus B = A\bar{B} + \bar{A}B = A\bar{B} + \bar{A}B + A\bar{A} + \bar{B}B$$

$$= A\,(\bar{A} + \bar{B}) + B\,(\bar{A} + \bar{B}) \tag{2.5}$$

By applying the principle of double negation and De Morgan, we get:

$$Y = A\,(\overline{AB}) + B\,(\overline{AB}) = \overline{(\overline{A\,(\overline{AB})} \;+\; \overline{B\,(\overline{AB})})}$$

$$= \overline{[\overline{A\,(\overline{AB})}][\overline{B\,(\overline{AB})}]} \tag{2.6}$$

Which implementation takes us to the following circuit (economic way of implementing XOR):

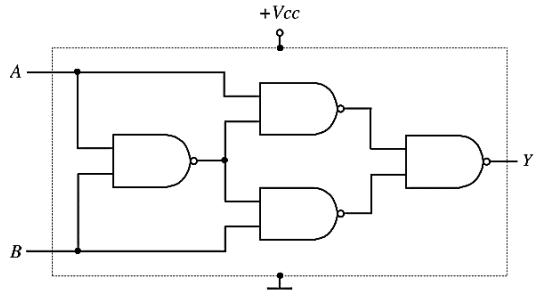


Figure 18. XOR scheme with NAND gates

With 4 NAND gates the XOR function can be implemented using a CBD400. Using the appendices, we can number the pins:

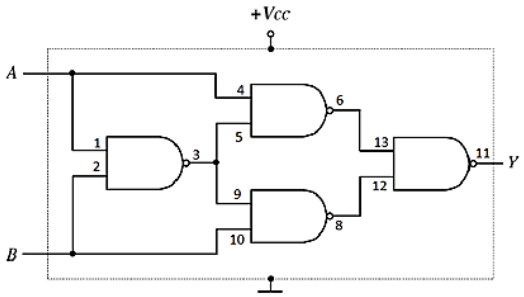


Figure 19. XOR scheme with using a CBD400 gates